V^2I_C Control: a Novel Control Technique with Very Fast Response Under Load and Voltage Steps

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***Abstract*— High switching frequencies (several MHz) allow the integration of low power DC/DC converters. Although, in theory, a high switching frequency would make possible to implement a conventional voltage mode control with very high bandwidth, in practice, parasitic effects and robustness make very complex to achieve bandwidths higher than 1MHz. This paper proposes a fast control technique to optimize the dynamic response of high switching frequency DC/DC converters. The proposed control is based on two loops. The fast internal loop has information of the output capacitor current and the error voltage, providing fast dynamic response under load and output voltage reference steps, while the slow external voltage loop provides accurate steady state regulation. Experimental results validate the fast dynamic response of the proposed control under load and output voltage reference steps and its suitability for high switching frequencies.**

I. INTRODUCTION

Nowadays, power supplies for powering microprocessors and portable devices require fast dynamic response under load and output voltage steps. This can be achieved by a conventional linear control with a high bandwidth. This high bandwidth is limited either by the switching frequency or by the robustness of the known system dynamics at high switching frequency. Other solutions are non-linear controls or combination of non-linear and linear control.

Well known non-linear strategies are V^2 ([1], [2] and [3]) or hysteretic control of the output voltage [3]. Both require sensing the output voltage ripple, which is very small compared to the DC value and it is very sensitive to parasitic effects. It is also required to have a triangular output voltage ripple given by a dominant ESR in the output capacitor, not suitable for good capacitors.

The combination of non-linear and linear control proposed in [4] is based on a hysteretic control of the output capacitor current of a Buck converter. It achieves a faster control action under load steps since the output capacitor current reacts instantaneously. The problem is to measure the output capacitor current but it can be estimated with the non-invasive method described in [5]. However, this method suffers some limitations: variable frequency and high sensitivity to current sensor mismatches.

The fast control technique proposed in [6] and implemented in [7] with the capacitor current estimator of [5] provides good transient response with constant switching frequency and low sensitivity to parasitic effects. Since it is based on the peak current mode control of the output capacitor current and it works as a feed-forward of the load current [8], it achieves fast dynamic response under load steps. However, the response of this control under changes in the output voltage reference is not so fast. The control proposed in this paper is based on this peak current mode control of the output capacitor current [7] but adding the error between the voltage reference and the output voltage in the fast loop. Thus, the dynamic response under changes in the voltage reference is improved and the fast dynamic response under load steps is still given by the output capacitor current measurement.

II. PROPOSED SOLUTION: V^2I_C CONTROL

A. Operating principle

The control proposed and analyzed in this paper is based on two loops, a fast internal loop and a slow external loop (Figure 1).

The control signal (Ctrl) obtained in the fast loop is the addition of: 1) the estimation of the output capacitor current measured with the non-invasive sensor described in [5], 2) the error between the voltage reference (V_{ref}) and the output voltage (V_{out}) and 3) a compensating slope. This control signal is compared with the reference (Ref) obtained in the slow external loop at the output of a voltage regulator.

The modulator used is a peak mode control and therefore a compensating slope is needed to avoid sub-harmonic oscillations over 50% duty cycles. The compensating slope not only avoids sub-harmonic oscillations, but also helps to desensitize this technique to current sensor mismatches and

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parasitic effects. On the other hand, increasing the compensating slope, the dynamic response is reduced. Therefore, there is a trade-off between stability and dynamic response.

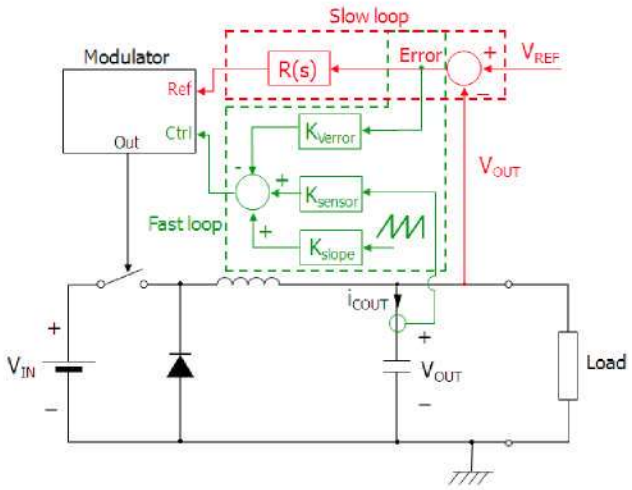

Figure 1. Proposed technique: V^2I_C control.

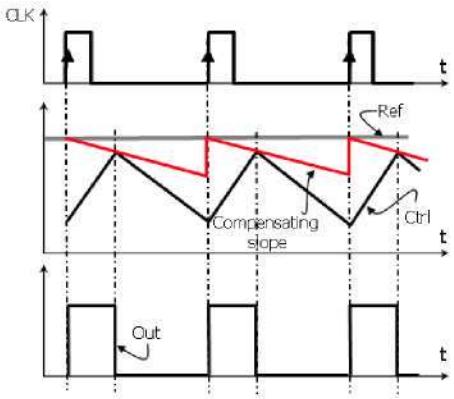

Figure 2. Proposed control operating principle.

The modulator used works as a peak current mode control. The main switch is turned on every cycle, thanks to a RS latch, and turned off when the control signal reaches the reference (Figure 2). Hence, this control technique prevents from the problem of variable frequency. The output capacitor current measurement provides fast dynamic response to load transitions since it behaves as a feed-forward of the load current and any change is instantaneously reflected in the control signal (Ctrl). When a positive load step occurs, the output capacitor current goes down almost immediately and therefore the control signal goes down as well. The duty cycle is saturated until the control signal reaches the reference again (Figure 3). On the other hand, the output error voltage feedback improves the dynamic response under changes in the output voltage reference as it is reflected in the control signal (Ctrl) and in the reference signal (Ref) (Figure 4). Finally, the external voltage loop provides accurate steady state regulation.

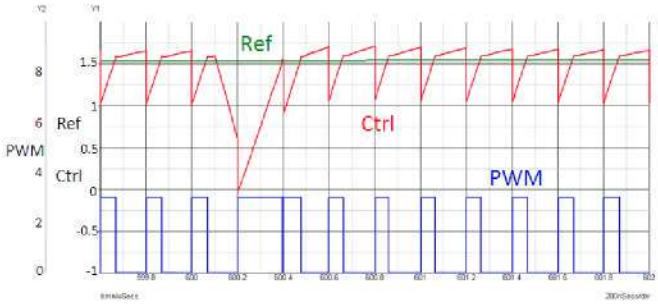

Figure 3. Control response under load step (4A) of 40A/µs. Reference signal Ref (500mV/div), control signal Ctrl (500mV/div) and gate signal PWM (1.67V/div) with 200ns/div time scale.

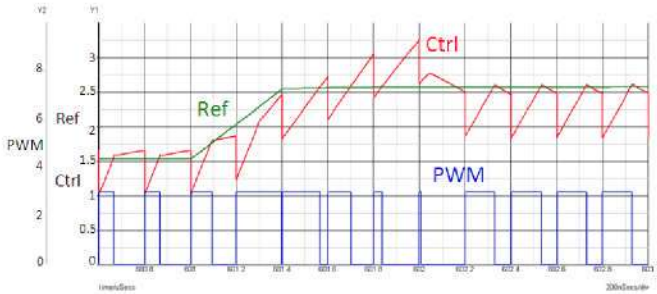

Figure 4. Control response under output voltage reference step (from 1V to 2V) of 2.5V/µs. Reference signal Ref (500mV/div), control signal Ctrl (500mV/div) and gate signal PWM (1.43V/div) with 200ns/div time scale.

The proposed control is called V^2I_C control since the output voltage is used in both fast and slow loops (V^2) and the output capacitor current (I_C) is also used in the fast loop.

The modulator in Figure 1 can be a peak control modulator but also other modulators could be used like valley peak, constant on-time, constant off-time or hysteretic control.

B. Design example

As a design example the following specifications have been chosen for the power stage: V_{in}=3V, V_{out}=1V, f_{sw}=5MHz, L=100nH and C_{out}=4µF. The compensating slope peak to peak amplitude is 600mV. The error voltage loop gain (K_{Verror}) is 1 while the current loop gain (K_{sensor}) is 0.2V/A. The purpose of these gains is to reduce the capacitor current ripple, since it is much higher than the output voltage ripple.

The SIMPLIS simulation tool is used to obtain the frequency response of the system and to design the external voltage loop, since it provides a fast way to obtain the desired transfer function. In Figure 5 the reference (Ref) to output voltage (V_{out}) frequency response is shown. In Figure 6 the output impedance is shown with a) the fast and slow loops open and with b) the fast loop closed and the slow

loop open. It can be seen how the output impedance is improved closing the fast loop (the output impedance is at least reduced in 12dB).

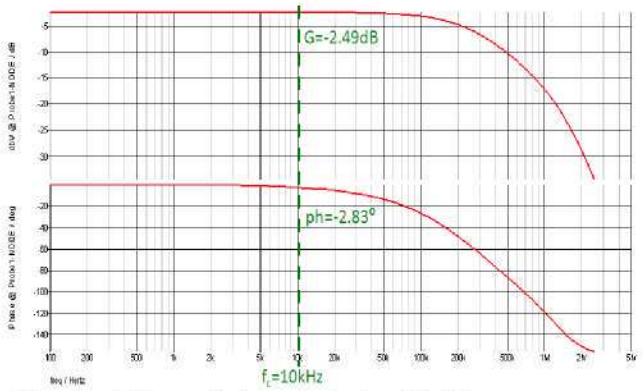

Figure 5. Reference (Ref) to output voltage (V_{out}) frequency response.

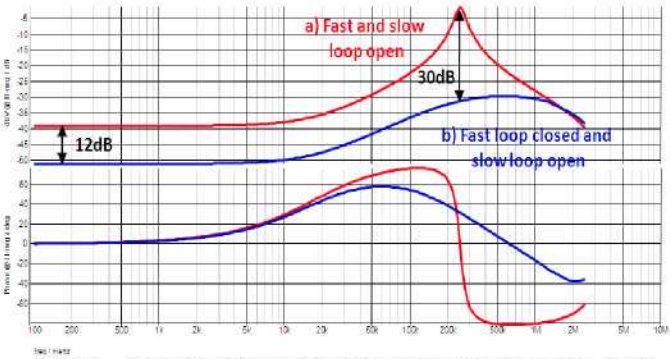

Figure 6. Output impedance with a) the fast and slow loops open and b) the fast loop closed and the slow loop open.

The external voltage loop has been designed with a bandwidth of 10kHz. The output voltage and inductance current responses in closed loop under load step are shown in Figure 7 and Figure 8. The output voltage needs only 3µs to recover the steady state and the voltage drop is of 180mV. The inductance current reacts rapidly following the reference with high slew rate.

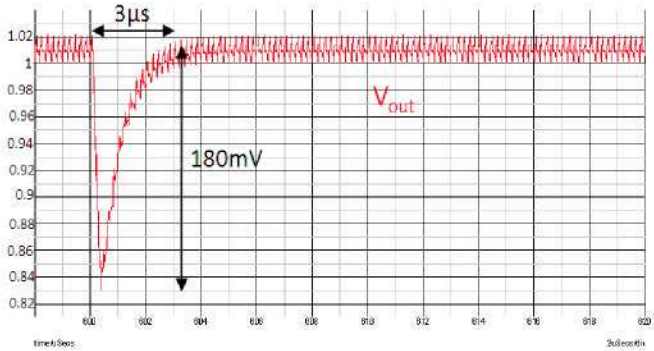

Figure 7. Response under positive load step of 4A (40A/µs). Output voltage V_{out} (20mV/div) and 2µs/div time scale.

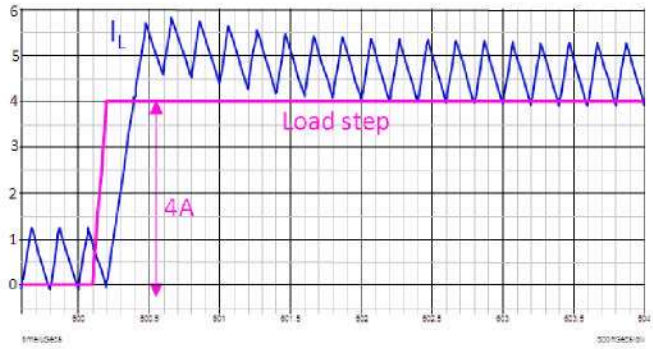

Figure 8. Response under load step of 4A (40A/µs). Inductance current I_L (1A/div) and 2µs/div time scale.

The output voltage response under output voltage reference step is shown in Figure 9. The output voltage follows the reference with accuracy and without overshoot.

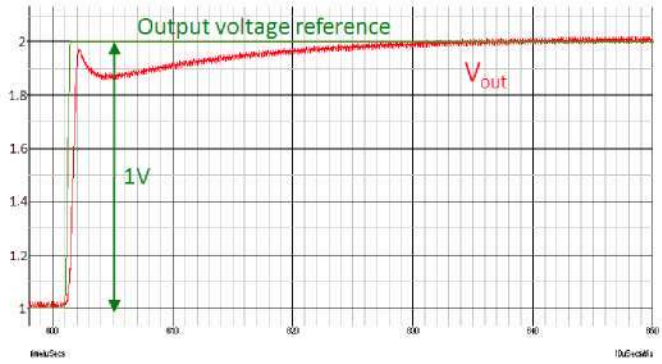

Figure 9. Response under positive output voltage reference step of 1V (2.5V/µs). Output voltage V_{out} (200mV/div) and 10µs/div time scale.

Finally, in Figure 10 and Figure 11 the closed loop gain and output impedances are shown.

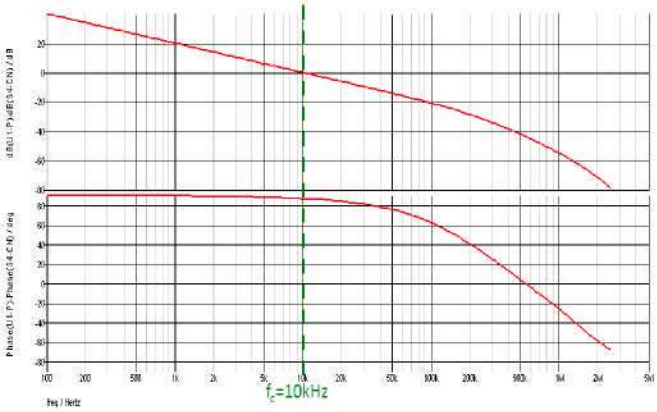

Figure 10. Closed loop gain.

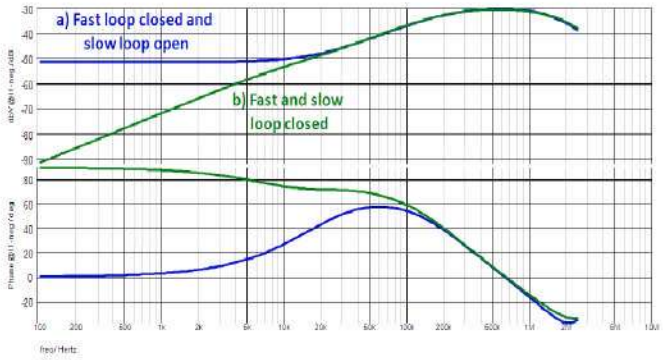

Figure 11. Output impedance with a) the fast loop closed and the slow loop open and b) the fast and slow loops closed.

III. V^2I_C CONTROL: DYNAMIC RESPONSE COMPARISON

In order to demonstrate the fast dynamic response of the proposed control it has been compared with the following control techniques:

- Peak current mode control of the output capacitor current [7].
- High bandwidth voltage mode control.
- V^2 control.

The external voltage loop of the proposed control has been designed with the simulation tool SIMPLIS. The control is applied to a buck converter with the following specifications: V_{in}=3V, V_{out}=1V, f_{sw}=1MHz, L=440nH, C_{out}=4µF and ESR=4.8mΩ. The external voltage loop bandwidth selected for the proposed control and the peak current mode control of the output capacitor current is 10kHz, and for the voltage mode control is 300kHz, in order to achieve a similar dynamic response to the proposed control.

Under load steps (Figure 12) the proposed control is faster than the peak current mode control of the output capacitor current with the same voltage drop. Compared with the voltage mode control, the proposed control provides the same response even though the bandwidth is 30 times lower.

Under output voltage reference steps (Figure 13), the voltage mode control and the peak current mode control of the output capacitor current responses show a large overshoot. However, the proposed control has a very good response under voltage reference steps following with high accuracy the reference. This fast response is produced thanks to the error voltage feedback in the control.

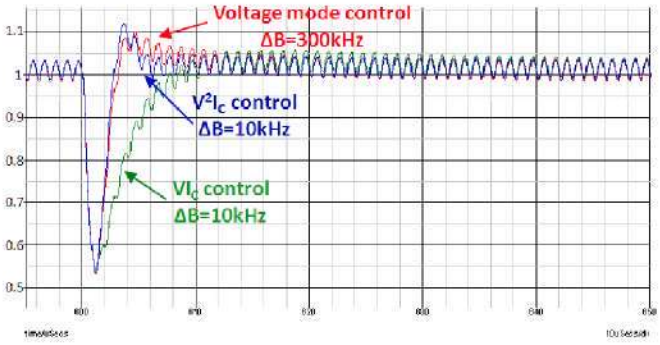

Figure 12 Response under positive load step of 4A (40A/µs). Output voltage (100mV/div) and 10µs/div time scale.

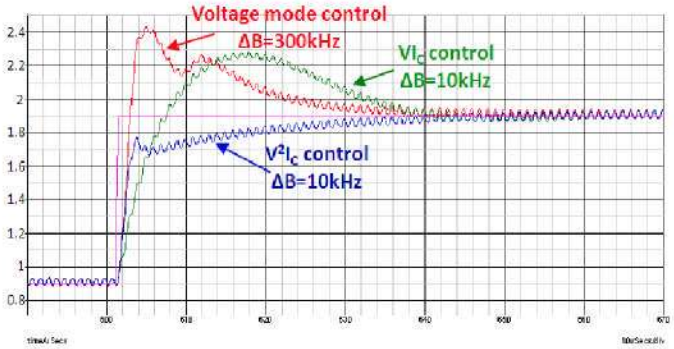

Figure 13. Response under positive output voltage reference step of 1V (2.5V/µs). Output voltage (200mV/div) and 10µs/div time scale.

If the V^2I_C control is compared now with the V^2 control with the same bandwidth, it can be seen in Figure 14 and Figure 15, under load and voltage reference step, how V^2 control presents oscillations, even though a compensating slope has been added to the V^2 control [2]. These oscillations are due to the non-dominant ESR in the output capacitor. Hence, the proposed control has the advantage of insensitivity to non-dominant ESR.

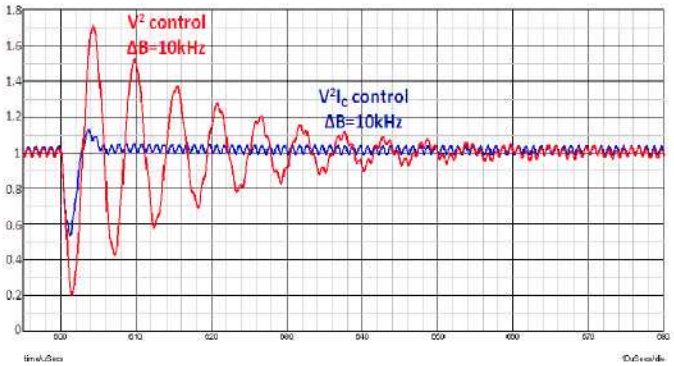

Figure 14. Response under positive load step of 4A (40A/µs). Output voltage (200mV/div) and 10µs/div time scale.

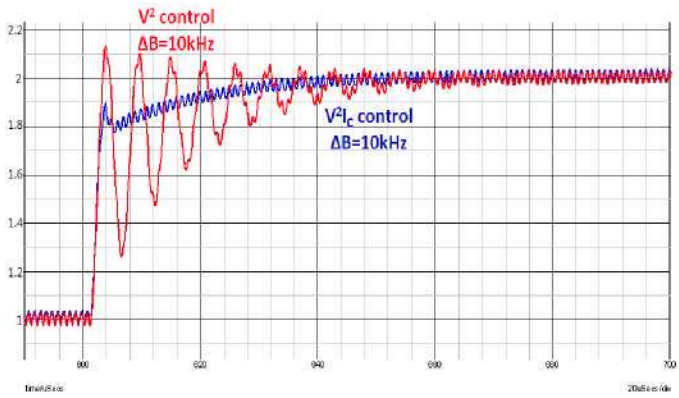

Figure 15 Response under positive output voltage reference step of 1V (2.5V/µs). Output voltage (200mV/div) and 20µs/div time scale.

In conclusion, the proposed V^2I_C control in a buck converter switching at 1MHz and with an external voltage loop with a bandwidth of 10kHz has a better response than a voltage mode control with an external voltage loop with a bandwidth of 300kHz. Also the V^2I_C control presents a better response than a V^2 control, with the same bandwidth, in the case of using an output capacitor with non-dominant ESR.

In integrated DC/DC converters applications, in which a high switching frequency is needed, the comparison is more interesting. In this case the specifications are the following: V_{in}=3V, V_{out}=1V, f_{sw}=5MHz, L=100nH and C_{out}=4µF and ESR=4.8mΩ. The external voltage loop bandwidth of the proposed control and the peak current mode control of the output capacitor current is 10 kHz again, and for the voltage mode control is 1MHz, the one needed to achieve a similar dynamic response to the proposed control. In Figure 16 and Figure 17 the output voltage responses under load step and output voltage reference step are shown. The conclusions considering the dynamic response with a switching frequency of 5MHz are the same as with the switching frequency of 1MHz. The problem with the switching frequency of 5MHz is that in the voltage mode control a bandwidth of 1MHz is needed while the proposed control only needs 10kHz. This 1MHz bandwidth is difficult to implement due to robustness and parasitic effects. In addition, at high switching frequencies, the maximum bandwidth is limited by the output capacitor parasitic components and tolerances. In these applications the use of the proposed V^2I_C control would be very interesting.

At a switching frequency of 5MHz a V^2 control would also present oscillations under load and voltage reference steps, due to the non-dominant ESR.

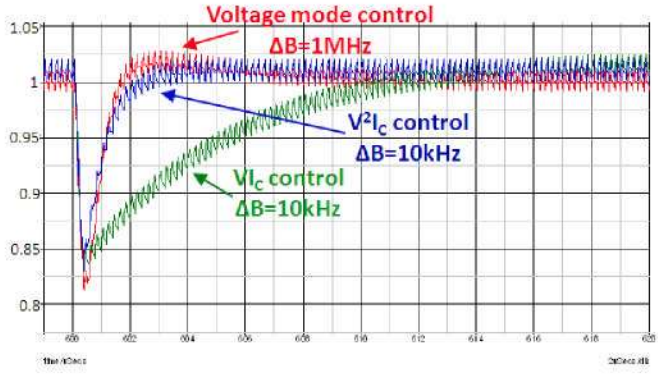

Figure 16. Response under positive load step of 4A (40A/µs). Output voltage (50mV/div) and 2µs/div time scale.

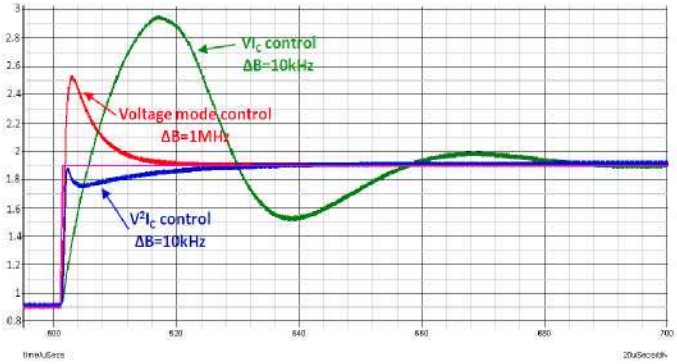

Figure 17. Response under positive output voltage reference step of 1V (2.5V/µs). Output voltage (200mV/div) and 20µs/div time scale.

IV. Experimental Results

The experimental results have been obtained on a buck converter being V_{in}=3V, V_{out}=1V, f_{sw}=1MHz, L=440nH and C_{out}=4µF and an external voltage loop designed for 10kHz.

The dynamic responses of the proposed control under positive and negative load steps are shown in Figure 18 and Figure 19. The control reacts almost immediately closing (Figure 18) or keeping open the main MOSFET (Figure 19). The inductance current follows the reference with high slew rate. The recovery time is only 3µs (three switching cycles).

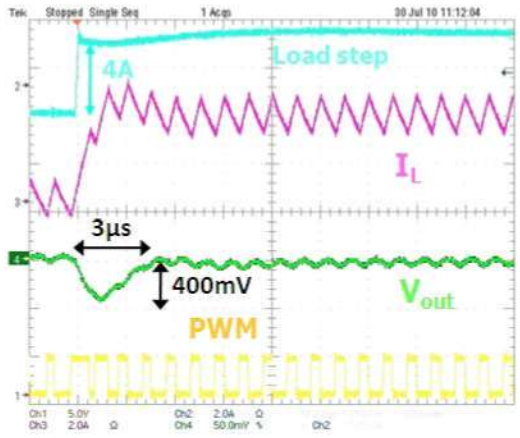

Figure 18. Experimental results. Positive load step of 1A and 40A/µs (2A/div), inductor current I_L (2A/div), output voltage V_{out} (500mV/div) and gate signal (5V/div) with 2µs/div time scale.

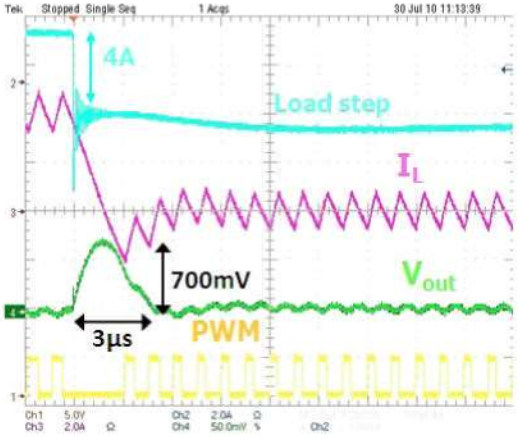

Figure 19. Experimental results. Negative load step of 1A and 40A/µs (2A/div), inductor current I_L (2A/div), output voltage V_{out} (500mV/div) and gate signal (5V/div) with 2µs/div time scale.

In Figure 20 and Figure 21 the experimental results obtained under positive and negative voltage reference steps are shown. The voltage reference step is done from 0.9V to 1.9V and vice versa. The control reacts almost instantaneously needing only two switching cycles to reach the new operating point and then, the external voltage loop provides the accurate steady state regulation. In addition, there is no overshoot in the output voltage due to the transient response.

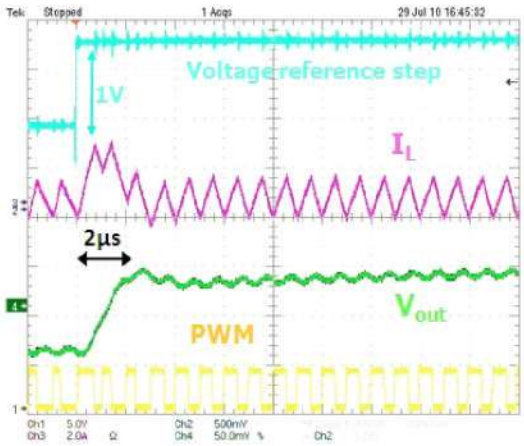

Figure 20. Experimental results. Positive voltage reference step of 1V and 20V/µs (500m/div), inductor current I_L (2A/div), output voltage V_{out} (500mV/div) and gate signal (5V/div) with 2µs/div time scale.

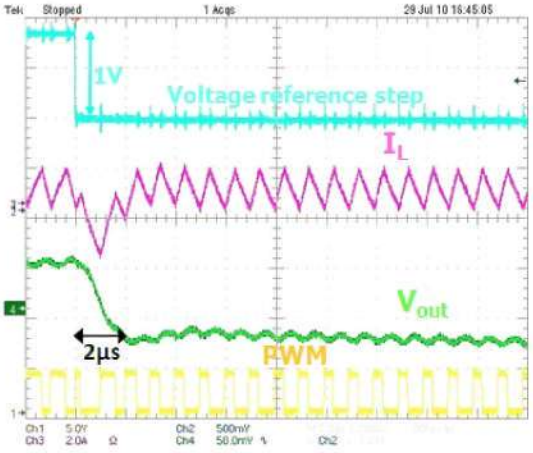

Figure 21. Experimental results. Negative voltage reference step of 1V and 20V/µs (500m/div), inductor current I_L (2A/div), output voltage V_{out} (500mV/div) and gate signal (5V/div) with 2µs/div time scale.

V. CONCLUSIONS

The V^2I_C control proposed and analyzed in this paper is based on two loops, a fast internal loop and a slow external loop. The control signal (Ctrl) obtained in the fast loop is the weighted addition of the estimation of the output capacitor current, the error between the output voltage reference and the output voltage and a compensating slope to avoid sub-harmonic oscillations. The control proposed is based on a peak mode control of this control signal (Ctrl). If a load or reference voltage change occurs it is instantaneously reflected in the control signal, giving fast dynamic response under load and output voltage reference steps. Finally the slow external loop provides accurate steady state regulation with low bandwidth required.

The advantages of this control are: 1) constant switching frequency, 2) fast dynamic response under load and output voltage reference steps and 3) low sensitivity to parasitic

effects and current sensor mismatches thanks to the slope compensation.

Finally, experimental results have been obtained in a buck converter switching at a frequency of 1MHz, verifying the fast dynamic response of the proposed control under load and output voltage reference steps. In both situations the control reacts almost immediately, thanks to the output capacitor current measurement and the error voltage feedback, achieving fast recovery times.

This control is very appropriate for very high switching frequencies (5MHz) integrated converters that need to achieve fast dynamic response under both load and output voltage reference steps. In these applications a bandwidth of about 1MHz would allow to optimize the dynamic response with a standard voltage mode control. However, 1MHz bandwidth is really complex to achieve due to parasitic effects. On the other hand, a V^2 control is not an appropriate alternative for an output capacitor with non-dominant ESR. The proposed V^2I_C control is a very interesting solution for this type of applications.

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